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2001-0673

PATTERN FOR MONITORING EPITAXIAL LAYER WASHOUT

FIELD OF THE INVENTION

001 This invention relates generally to semiconductor processing, and more particularly to monitoring epitaxial layer washout within such processing.

BACKGROUND OF THE INVENTION

002 Patterning is one of the basic steps performed in semiconductor processing. It also referred to as photolithography, masking, oxide or metal removal, and microlithography. Patterning enables the selective removal of material deposited on a semiconductor substrate, or wafer, as a result of a deposition process. For example, as shown in FIG. 1A, a layer 104 has been deposited on a substrate 102. After the photolithography process is performed, as shown in FIG. 1B, some parts of the layer 104 have been selectively removed, such that gaps 106a and 106b are present within the layer 104. A photomask, or pattern, is used (not shown in FIG. 1B) so that only the material from the gaps 106a and 106b are removed, and not the other portions of the layer 104. The process of adding layers and removing selective

parts of them, in conjunction with other processes, permits the fabrication of semiconductor devices.

003 Alignment is critical in photolithography and deposition, as well as in other semiconductor processes. If layers are not deposited properly, or if they are not selectively removed properly, the resulting semiconductor devices may not function, relegating them to scrap, which can be costly. Such misalignment, or overlay shift, is shown in FIG. 2. The layer 204 may or may not be deposited in a properly aligned configuration on the substrate 202, whereas subsequent deposition layers 206a, 206b, . . ., 206n are misaligned. This is indicated by the reference marks 210a, 210b, . . ., 210n, which are shown in FIG. 2 for illustrative clarity only. The reference marks 210a, 210b, . . ., 210n, should substantially align over the alignment marks 208 of the substrate 202, but they do not.

004 In comparison to FIG. 2, correctly aligned layers are shown in FIG. 3. The semiconductor wafer 202 has alignment marks 208. The layer 204 is aligned thereupon. Similarly, the layers 206a, 206b, . . ., 206n are deposited upon the layer 204, without

any, or with minimal, overlay shift. This is indicated by the reference marks 210a, 210b, . . ., 210n aligning with the alignment marks 208 of the wafer 202.

005 Specific types of alignment problems can result when using epitaxial layers grown over a semiconductor substrate. Epitaxy is the process in which a thin layer of a single crystal material is deposited on a substrate. Epitaxial growth occurs in such a way that the crystallographic structure of the substrate is reproduced in the growing material, although the conductivity and the doping level of the epitaxial layer can be independent of the underlying substrate layer. Silicon substrates with epitaxial layers are commonly used in complementary metal-oxide silicon (CMOS) semiconductor devices, bi-CMOS devices, high-voltage devices, and bipolar devices.

006 FIGs. 4A, 4B, and 4C show the alignment problems that can occur within a pattern in an epitaxial layer relative to the pattern in a substrate layer. In FIG. 4A, pattern shift has occurred. The pattern 406 in the substrate layer 402 has shifted to the right as the pattern 408 in the epitaxial, or epi, layer

404. In FIG. 4B, pattern distortion has occurred. The pattern 436 in the substrate layer 438 has become distorted as the pattern 438 in the epi layer 434. That is, the pattern 438 is smaller in width than the pattern 436 is. In FIG. 4C, pattern washout has occurred. The pattern 466 in the substrate layer 462 has washed out as the pattern 468 in the epi layer 464. These sorts of alignment problems can occur because of non-ideal deposition of the epi layers, and/or because of other improper processing. The patterns of FIGs. 4A, 4B, and 4C can be alignment marks, used for alignment in the subsequent processing of the epi layers and other layers.

007 When the alignment problems of FIGs. 4A, 4B, and 4C occur, adjustment must be made to the position of features on subsequent layers in order to compensate for the errors introduced in the epi layers. Selecting the correct amount of adjustment, however, is usually complicated by the fact that the effects are dependent on such varying factors as substrate orientation, deposition rate, deposition temperature, and silicon source. Furthermore, in the case of pattern washout of FIG. 4C in particular, subsequent processing performed relative to the

epi layer 464 will likely fail, because the semiconductor processing equipment will most likely not be able to align with the washed-out pattern 468. This alignment failure may be corrected by instead performing manual alignment, but this is a time-intensive and costly process.

008 Therefore, there is a need to be able to monitor epitaxial layer washout of alignment and other patterns. Such monitoring should be able to yield whether washout has occurred, so that it can be determined whether a given semiconductor wafer lot must be scrapped. Furthermore, such monitoring should be able to yield at what feature size washout has occurred, so that only the minimum number of semiconductor wafers is scrapped. For these and other reasons, there is a need for the present invention.

SUMMARY OF THE INVENTION

009 The invention relates to a pattern for monitoring epitaxial layer washout. The pattern includes first and second sub-patterns. The first sub-pattern has a shape and defines one or more minimum dimensions. Obfuscation of the first sub-pattern

means that epitaxial washout has occurred at least for dimensions equal to or less than the minimum dimensions. The second sub-pattern has the same shape of the first sub-pattern, but defines one or more maximum dimensions. Obfuscation of the second sub-pattern means that epitaxial washout has occurred for dimensions equal to or less than the maximum dimensions.

0010 The invention provides for advantages over the prior art. A series of sub-patterns may have decreasing dimensions at regular intervals. By proceeding down the series of sub-patterns, and determining the first sub-pattern of the series that is not clear - that is, which is obfuscated - a semiconductor technician can easily determine at which dimensions epitaxial layer washout has occurred. These dimensions are those that are equal to or less than the dimensions of the first sub-pattern of the series that is obfuscated. These dimensions can be referred to as the washout values for the epitaxial layer, and can include different horizontal and vertical dimensions, and hence washout values.

0011 Still other advantages, embodiments, and aspects of the invention will become apparent by reading the detailed description that follows, and by referencing the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

0012 FIGs. 1A and 1B are diagrams showing the effect of patterning on a layer deposited on a semiconductor wafer.

0013 FIG. 2 is a diagram showing the overlay shift that results when depositing and exposing subsequent layers on a layer deposited on a semiconductor wafer.

0014 FIG. 3 is a diagram showing, in comparison to that of FIG. 2, how multiple deposited and exposed layers without overlay shift appear on a semiconductor wafer.

0015 FIGs. 4A, 4B, and 4C are diagrams of pattern shift, pattern distortion, and pattern washout, respectively, that can problematically occur in epitaxial layers.

0016 FIG. 5 is a diagram of a pattern including a series of sub-patterns, by which monitoring of epitaxial layer washout can be accomplished, according to an embodiment of the invention.

0017 FIG. 6 is a diagram showing one of the sub-patterns of FIG. 5 in more detail, according to an embodiment of the invention.

0018 FIG. 7 is a flowchart of a method for monitoring epitaxial layer washout, according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

0019 In the following detailed description of exemplary embodiments of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific exemplary embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized, and logical, mechanical, and other changes may be made without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

0020 FIG. 5 shows a semiconductor pattern 500 for monitoring epitaxial layer washout. The pattern 500 is patterned on an epitaxial layer over a semiconductor substrate layer of a semiconductor wafer. For example, it may be patterned within the scribe lines of a wafer. Furthermore, there may be five sets of the pattern 500 within a given semiconductor mask. The pattern

has a width 510 and a height 512, which can in one embodiment be equal to 1800 micron and 80 micron, respectively.

0021 The pattern 500 includes a series of sub-patterns 502a . . . 502n. Preferably, there are twelve such sub-patterns, including the sub-patterns 502a and 502n, where the dotted line 504 represents ten additional intermediary sub-patterns. The dimensions of the series of sub-patterns 502a . . . 502n can be between 0.5 and 6.0 micron, increasing from the minimum of 0.5 for the sub-pattern 502a to the maximum of 6.0 for the sub-pattern 502n at regular intervals of 0.5 micron, such that the sub-patterns are uniformly spaced. The sub-pattern 502a has a given shape, and defines one or more minimum dimensions. After patterning on the epitaxial layer, if the sub-pattern 502a is obfuscated, this means that epitaxial washout has occurred for features having a size equal to or less than these minimum dimensions. The sub-pattern 502a specifically includes the separated features 506a and 506b.

0022 The sub-pattern 502n has the same general shape as the sub-pattern 502a, and defines one or more maximum dimensions. After patterning on the epitaxial layer, if the sub-pattern 502n is obfuscated, this means that epitaxial washout has occurred for features having a size equal to or less than these maximum dimensions. The sub-pattern 502n specifically includes the separated features 506a and 506b. Similarly, the intermediary sub-patterns represented by the dotted line 504 each has the same general shape as the sub-pattern 502a, and defines one or more intermediary dimensions. After patterning on the epitaxial layer, if a given sub-pattern is obfuscated, this means that epitaxial washout has occurred for features having a size equal to or less than its intermediary dimensions.

0023 FIG. 6 shows one of the sub-patterns of FIG. 5 in more detail, as the sub-pattern 600. The sub-pattern 600 includes features 602 and 604. The features 602 and 604 are interlocked or complementary, but separated, features, the latter in that they do not touch one another. As shown in FIG. 6, each of the features 602 and 604 is substantially L-shaped, in that each has two segments forming an L-shape. Preferably, each of the

features 602 and 604 has the same size and is thus identical in shape, such that the feature 604 represents a 180-degree rotation of the feature 602. The dimensions 606, 608, 610, and 612 of the features 602 and 604 can be 30 micron, 30 micron, 60 micron, and 60 micron, respectively, in one embodiment.

0024 The separation of the features 602 and 604 of the sub-pattern 600 defines the one or more dimensions defined by the sub-pattern 600. For instance, the dimension 614 is a horizontal dimension that separates the features 602 and 604, and specifically separates a vertical segment of the feature 602 from a horizontal segment of the feature 604. Similarly, and the dimension 616 is a vertical dimension that separates the features 602 and 604, and specifically separates a horizontal segment of the feature 602 from a vertical segment of the feature 604. A given sub-pattern 600 may thus have specific values for these dimensions 614 and 616, such as 4.0 micron for each. If after imprinting on the epitaxial layer the sub-pattern 600 is not clear - such that it is obfuscated - this indicates that feature dimensions of other features imprinted thereon of less than or equal to 4.0 micron will not be clear. That is, obfuscation

indicates that epitaxial washout has occurred at this and lesser-sized dimensions.

0025 FIG. 7 shows a method 700 for monitoring epitaxial layer washout. First, an epitaxial layer is deposited over a substrate layer of a semiconductor wafer (702). For example, the epitaxial layer may be grown over the substrate layer. A series of sub-patterns is then patterned on at least the epitaxial layer (704). The series of sub-patterns can be and is preferably the series 502n . . . 502a of FIG. 5. The series of sub-patterns defines progressively decreasing one or more dimensions, and this is why the series is indicated as the series 502n . . . 502a of FIG. 5, since such an ordering represents progressively decreasing dimensions.

0026 Next, the first obfuscated sub-pattern in the series is located (706), by starting at the sub-pattern having the maximum dimension(s), and proceeding through the series of sub-patterns and potentially to the sub-pattern having the minimum dimension(s). Finally, the washout values are set as the dimension(s) of this first obfuscated sub-pattern (708). These

washout values indicate the dimension(s) at which epitaxial washout has occurred, such that dimensions equal to or less than these values are concluded to be washed out on the epitaxial layer. Other features patterned on the epitaxial layer having dimensions equal to or less than the washout values are thus washed out, too.

0027 It is noted that, although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and equivalents thereof.